New Generation Solution for Micro Via Metallization and Through Hole Plating

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Abstract
Smaller holes and increasing circuit density are drivers that push technology for via in pad and stacked microvia designs that help minimize PWB real estate. It has been established that via in pad designs, where the via is not filled, can lead to voids in the BGA solder joint which can negatively affect reliability.
Stacked vias, or sequential build-up process is a known technology where vias (either blind or through hole) are metallized, plated to required thickness then circuitized. Another layer of dielectric is applied and the process repeated.
This paper discusses a vertical, direct current (DC) acid copper electroplating system that achieves filling and excellent physical properties of the deposited copper. The copper electrolyte is based on sulfuric acid. This process exhibits stable, long-term performance and possesses a wide operating window that incorporates a new approach to accelerate the bottom up filling mechanism. A wide range of working current densities can be utilized, thus permitting for a flexible plating time dependent on board design. The throwing power of the plating solution as well as the mechanical properties of the electroplated copper are studied. The filling capabilities described enable a highly reliable stacked via construction.

Introduction

Increased packaging functionality and increased pitch density have been required to address the need of smaller and more capable electronic devices. Micro via constructions assist in meeting these requirements. Newer designs incorporate the filling of these vias.
Electro-deposited copper is becoming the preferred method of filling microvias, replacing the alternative via filling techniques especially as the conductor patterns become finer and pitch density of the component packaging increases. Resin or conductive pastes have been used for via filling, however the reliability problems associated with these materials include subsequent polishing, entrapped air within the blind micro via and void formation during the reflow process. Electroplating is a highly preferred method, due to its high deposition rate, the ability to fill deep micrometer & sub-micrometer features, low cost of the process, and superior conductivity [1]. Electrolytically filling the vias eliminates the steps involved in screening a via fill, curing and planarizing. Copper filled vias can assist in the heat dissipation in PWB’s due to the heat sinking capacity of copper. Filling the laser-drilled microvia using electrolytic copper enables stacked via technology, which further reduces required circuitry [2,3].
The trends in via sizes are given in Table 1.

<u>Table 1. Trend in the Blind Micro-via size</u>

	2004 - 2005	2006 - 2007	2008 - 2009	2010 - 2014
Via Size (µm)	60 - 150	50 - 125	40 -100	30 - 80
Via pitch (µm)	200- 600	180 -500	150 -400	125 - 325
Blind Via Aspect Ratio	0.8 – 1.0	0.9 – 1.1	1.0 –1.2	1.0 – 1.3

Future designs will incorporate smaller diameter vias, and increasing aspect ratios. Meeting the future challenges will require a refinement of the existing process through tighter control of the organic additive concentrations in the plating solution, multiple plating operations or equipment modifications.

The requirements for HDI boards include highly efficient micro via filling and excellent physical properties of the plated through holes (PTH) in the same board. No corner cracks should occur during the standard thermal shock tests. Throwing power of the electrolyte has to allow for sufficient copper thickness within the through hole, which is at least 20 m (0.8 mils) as of current specification.

Simultaneously via filling and reliable through hole metallization could not be achieved using conventional copper plating technology. The size / aspect ratio of the blind micro-vias that could be filled with copper using these technologies are limited. The long-term performance of such electrolytes is not satisfactory.

In this paper a vertical direct current (DC) acid copper electroplating process for both micro via filling and through-hole metallization is described. An acid copper electrolyte, comprised of either alkanesulfonic acid or sulfuric acid is used. Bottom up filling mechanism is enhanced by preliminary treatment of the boards in a proprietary solution. The process has been successfully demonstrated in a production environment.

Test Vehicles to Develop the Process

Test vehicles for measuring filling capability were of 2 designs. Both designs employed a CO_2 laser for drilling the vias. The first test vehicle utilized glass reinforced dielectric (prepreg). Via diameters were 75 m, 100 m, 125 m, 150 m, and 175 m, and depths were 75 m, and 100 m. Via sizes were varied in a 4"x 4" grid pattern, which enabled a large range of diameters and depths to be plated simultaneously. A second test vehicle was constructed employing resin coated copper (RCC) with 100, 125, 150 and 175µm diameter vias with a depth of 75µm.
The test vehicles were processed through a standard permanganate desmear cycle, followed by a medium deposition electroless copper process. Alternative forms of primary metallization were tested, (specifically conductive polymer and a carbon direct metallization technology), but were not part of the capability study.
The test vehicle for measuring plated through hole performance was a 1.6mm thick panel with 0.50 mm, 0.35 mm, 0.25mm and 0.20mm holes.
Although alkanesulfonic acid exhibit some benefits for the wetting of small vias, however the increased cost may not be justified when plating microvias of 75 micron diameter or larger. In this study sulfuric acid electrolytes of various compositions were screened. Organic plating additives are an essential component in the plating bath. Various organic species were evaluated for suppression and anti-suppression properties. Compounds containing amino groups were added as leveler agents.
The final selection was based on the ability of the system to effectively fill micro vias while simultaneously plating through holes with a copper deposit possessing very good mechanical properties. A further enhancement of the process was to incorporate a predip containing a so-called promoter that accelerates plating rate. Various species and concentrations were evaluated, and the parameters optimized.
The immersion of the test vehicles in a solution containing plating promoter, results in its' adsorption over the primary metallization coating. Board movement and/or solution agitation allow for penetration of the solution into the vias and accumulation of the accelerator on the side

walls and via bottom. During the subsequent operations, the accelerator is preferably removed from the outer surface. This approach creates different conditions for copper plating within the vias verses the surface of the panel.
Utilizing the process with a pre-dip treatment a wide range of organic additive concentrations in the electrolyte is tolerable. The process is not sensitive to variations in additive concentration and it is easier to control. Improved metal properties could be achieved by reducing or eliminating some of the organic components of the electrolyte. Via fill plating is predictable and consistent for a large variety of via sizes, including small diameter vias and higher aspect ratios. Minimized thickness and thickness variations across the substrate surface is achieved.
The optimum electrolyte composition and the process parameters are shown in Table 2.

Table 2. Electrolyte Composition and Process Parameters

Component	Target	Range
Cu as metal	50 g/L	40 - 55g/L
Free Sulfuric Acid	100 g/L	90 - 110 g/L
Cl^-	75 ppm	60 -80 ppm
MacuSpec VF 100 Wetter	9 mL/L	8 – 12 mL/L
MacuSpec VF 100 Brightener	4.5 mL/L	1.5 – 6 mL/L
MacuSpec VF 100 Leveler	8 mL/L	6 - 15 mL/L
Current Density	1.0 – 2.0 A/dm^2	0.5 –3.0 A/dm^2
Temperature	21 - 22°C	20 – 24°C
Preliminary Treatment solution	10% 21 - 22°C	8-12% 20 – 28°C

Plating time depends on via size being plated and the current density used. In general, larger diameter microvias require higher current density to maintain reasonable plating cycle times. Current ramping was utilized in order to achieve consistent void free plating for high aspect ration vias, 1:1 and higher as well as for dimple minimization filling of large diameter vias. The ramping regimes varied depending on via size and plating time limitation.

Evaluation of the Plated Test Vehicles

Standard cross-sectioning techniques were used to qualify filling capabilities and microdistribution in through holes. A fill ratio of 80% or greater was the metric used to determine filling success. See figure 1.
Fill Ratio = A/B x100

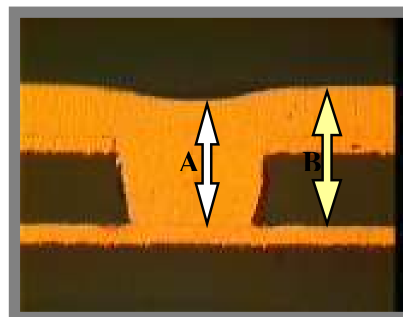


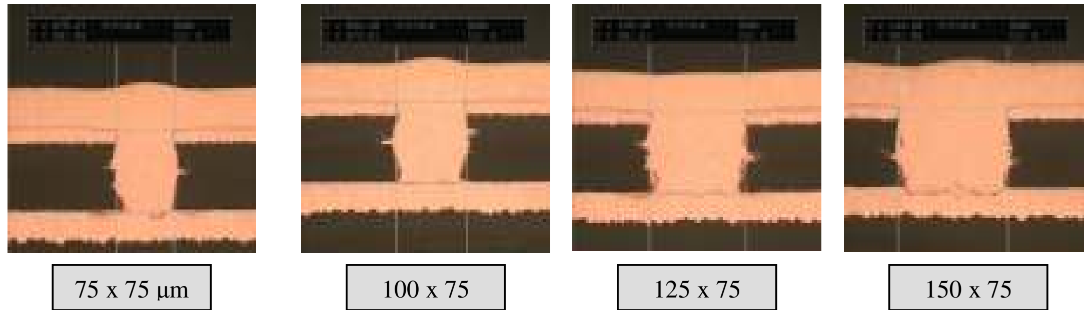
Figure 1.

Process Capabilities

The capabilities of the process are shown in Figure 2 and Figure 3. All test vehicles were plated with a moderate air agitation of about 2-3 l/min (Cole-Parmer airflow measuring gage) at 21 - 22°C. A large range of via sizes was plated with a fill ratio more than 80%, which is the acceptable fill ratio [4].

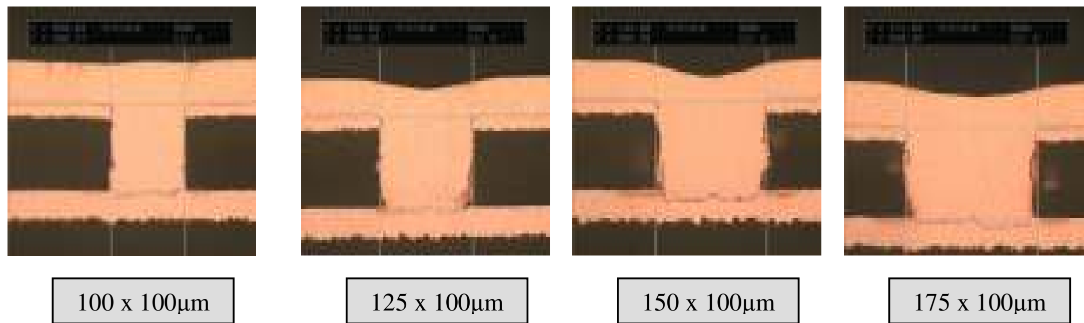
The process demonstrated an ability to fill 1:1 aspect ratio micro-vias without voids on both glass re-enforced dielectrics and resin coated copper. Since most production scale manufacturing utilizes glass re-enforced dielectric, this study concentrated on prepreg. Laboratory capabilities are shown in figures 2 and 3.

Figure 2



75 x 75 µm | 100 x 75 | 125 x 75 | 150 x 75

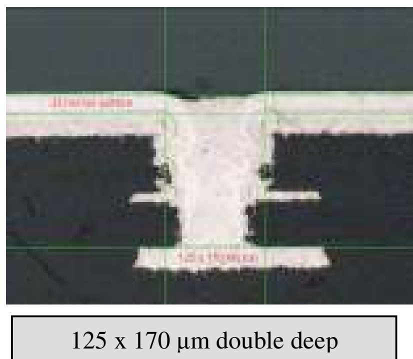
Figure 3



100 x 100µm | 125 x 100µm | 150 x 100µm | 175 x 100µm

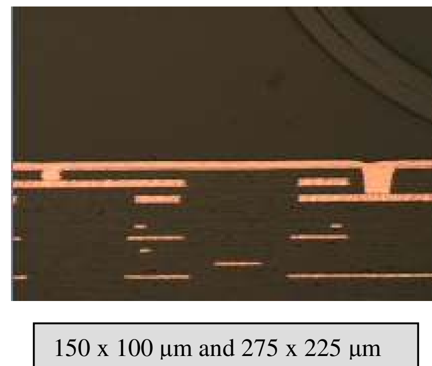
Production installations have shown a wider process capability. Double deep blind microvias can be filled. Multiple via sizes and depths can be filled on the same panel utilizing the same plating cycle. Production capabilities are shown in figures 4 and 5.

Figure 4



125 x 170 µm double deep

Figure 5



150 x 100 µm and 275 x 225 µm

Reliability Results

Reliability Test	Condition	Result
IPC TM 650-2.6.8	Solder shock 6x @288ºC	Pass: No cracks
IPC TM-650 2.4.18.1	Tensile strength, elongation	Pass 42kpsi; 20% elongation
L3 Preconditioning	JESD 22-A 113E (30ºC,60%RH, 192Hr, 150ºC)	Pass
TCT	-55ºC to 125ºC 1000 cycles	Pass
HAST	96 hr, 130ºC, 85% RH, 3.7V	Pass
PCT	96 hr, 2 atm, 121ºC, 100% RH	Pass

Conclusions and Discussion

A new technology for vertical direct current (DC) micro-via filling with simultaneous through hole copper plating has been developed based on sulfuric acid. An additional predip protects the plating bath and sets up a more efficient bottom filling process.

The technology has demonstrated the ability to fill a vast range of via sizes, including small diameter vias with aspect ratios in excess of 1:1.

Production installations have demonstrated the capability to maintain exceptional filling characteristics beyond 500 ampere hours per liter without any solution treatments required.

The physical-mechanical properties of the plated copper deposit are excellent.

Tensile strength and elongation properties exceed IPC specification, and the plated deposit meets IPC 6012A class 3 criteria for the plated through holes.
The current modulation/ramp opens the operating widow for the entire process. Further investigation is required to develop specific waveforms for different geometries and technologies.

Other waveforms, such as Periodic Pulse Reverse, Periodic Pulse and combinations therein are under evaluation to fill vias and enhance the throwing power on high aspect ratio through holes.

REFERNCES

1. Clyde F. Coombs Jr., *Printed Circuit Handbook*, Fifth edition, New York (2001).
2. J. H. Lau, *Low Cost Chip Technology for DCA, WLCSP, and PBGA Assemblies*, McGraw-Hil, Inc., New York (2000).
3. T. Kobayashi, J. Kawasaki, K. Mihara, and H. Honma, Electrochim. Acta, 47, 85 (2001).
4. M. Lefebre, G. Alladyce, M. Seita, H. Tsuchida, M. Kusaka, and S. Hayashi, S23-2-1, ICP Printed Circuit Expo (2004) USA.